Government of Karnataka
Department of Technical Education
Bengaluru

	Course Title: **Digital Electronics Lab**		
	Scheme (L:T:P) : **0:2:4**	Total Contact Hours: **78**	Course Code: **15EC03P**
	Type of Course: **Tutorial & Practical's**	Credit **:03**	Core/ Elective: **Core**
CIE- 25 Marks			SEE- 50 Marks

Prerequisites:

Knowledge of Basic Electronics Engineering in I – semester.

Course Objectives:

Students will learn and understand the Basics of digital electronics and able to design basic logic circuits, combinational and sequential circuits.

Course Outcome

On successful completion of the course, the students will be able to attain below Course Outcome (CO):

Course Outcome		Experiment linked	CL	Linked PO	Teaching Hrs
CO1	Identify the various digital ICs and understand their operation.	***1,2,3,4***	***R, U***	1,2,3,4,8,10	**18**
CO2	Apply Boolean laws to simplify the digital circuits.	***5,6***	***U, A***	1,2,3,4,8,10	**15**
CO3	Illustrate combinational logic circuits	***7,8,9***	***U, A***	1,2,3,4,8,10	**21**
CO4	Illustrate Sequential logic circuits	***10,11,12,13,14***	***U, A***	1,2,3,4,8,10	**24**
			Total sessions		**78**

Legends: R = Remember U= Understand; A= Apply and above levels (Bloom's revised taxonomy)

Course-PO Attainment Matrix

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
Digital and Computer fundamentals	**3**	**3**	**3**	**3**	**-**	**-**	**-**	**3**	**-**	**3**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.
If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3
If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2
If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1
If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.

List of Graded Exercises

1. Compare analog and digital electronics systems (Tutorial)
2. Realization of basic and universal logic gates using ICS 7400, 7432, 7402, 7408, 7486, 7404.
3. Realization of NOT, OR, AND, NOR, XOR, XNOR using NAND.
4. Realization of NOT, OR, AND, NAND, XOR, XNOR using NOR.
5. Verification of Demorgan's theorem.
6. Simplify the Boolean expression using Boolean algebra and verify.
7. Realization of half adder and full adder.
8. Verification of TT of 4:1 mux & 1:4 demux using IC's.
9. Interfacing 7-segment display system with IC 7447 to display 0-9
10. Verification of TT of flip flops
    (i) Clocked RS FF using NAND gate
    (ii) JK FF using IC 7476
    (iii) D- FF
    (iv) T-FF using JK Flip-flop
11. Verification of TT of shift registors (7495)
    (i) SISO
    (ii) SIPO
    (iii) PISO
    (iv) PIPO
12. Verification of 4-bit Asynchronous mod-10 (decade) counter (IC 7490)
13. Verification of 4-bit synchronous up/down counter ((IC 74193)
14. 4-bit Ring counter (Tutorial followed by experiment)

Course Delivery

The course will be delivered through tutorials of two hours and four hours of hands on practice per week.

Reference

1. Digital Fundamentals, Thomas L. Floyd, Pearson Education, ISBN:9788131734483
2. Digital Principles and Applications, Malvino and Leach, TMH

e-Resources

1. http://www.vlab.co.in/
2. http://www.asic-world.com/
3. http://electrical4u.com/
4. http://www.electronics-tutorials.ws

Course Assessment and Evaluation Scheme

Method	What		To whom	When/Where (Frequency in the course)	Max Marks	Evidence collected	Course outcomes
DIRECT ASSESSMENT	CIE (Continuous Internal Evaluation)	IA Tests	Students	Two IA Tests (Average of two tests will be computed)	10	Blue books	1,2,3,4
				Record Writing (Average marks of each exercise to be computed)	10	Record Book	1,2,3,4
				Student Activity	05	Log of record	1,2,3,4
				TOTAL	**25**		
	SEE (Semester End Examination)	End Exam		End of the course	50	Answer scripts at BTE	1,2,3,4
INDIRECT ASSESSMENT	Student Feedback on course		Students	Middle of the course		Feedback forms	1, 2,3,4 Delivery of course
	End of Course Survey			End of the course		Questionnaires	1,2,3, 4 Effectiveness of Delivery of instructions & Assessment Methods

***CIE** – Continuous Internal Evaluation ***SEE** – Semester End Examination

Note:

1. I.A. test shall be conducted as per SEE scheme of valuation. However obtained marks shall be reduced to 10 marks. Average marks of two tests shall be rounded off to the next higher digit.
2. Rubrics to be devised appropriately by the concerned faculty to assess Student activities.

Questions for CIE and SEE will be designed to evaluate the various educational components (Bloom's taxonomy) such as:

Sl. No	Bloom's Category	%
1	Remembrance	10
2	Understanding	20
3	Application	70

Format for Student Activity Assessment

DIMENSION	Unsatisfactory 1	Developing 2	Satisfactory 3	Good 4	Exemplary 5	Score
Collection of data	Does not collect any information relating to the topic	Collects very limited information ; some relate to the topic	Collects some basic information ; refer to the topic	Collects relevant information ; concerned to the topic	Collects a great deal of information ; all refer to the topic	3
Fulfill team's roles & duties	Does not perform any duties assigned to the team role	Performs very little duties	Performs nearly all duties	Performs all duties	Performs all duties of assigned team roles with presentation	4
Shares work equally	Always relies on others to do the work	Rarely does the assigned work; often needs reminding	Usually does the assigned work; rarely needs reminding	Does the assigned job without having to be reminded.	Always does the assigned work without having to be reminded and on given time frame	3
Listen to other Team mates	Is always talking; never allows anyone else to speak	Usually does most of the talking; rarely allows others to speak	Listens, but sometimes talk too much	Listens and contributes to the relevant topic	Listens and contributes precisely to the relevant topic and exhibit leadership qualities	3
					TOTAL	**13/4=3.2=4**

All student activities should be done in a group of 4-5 students with a team leader.

Scheme of Evaluation for End Exam

SN	Scheme	Max. Marks
1	Writing Circuit and Procedure of one Experiment	20
2	Conduction	15
3	Result	05
4	Viva voce	10
Total		**50**
Note: 1. Candidate shall submit Lab Record for the Examination. 2. Student shall be allowed to execute directly even if he / she unable to write the procedure 3. In case of change in experiment or no write up, marks will not be awarded for writing procedure/steps.		

Resource requirements for Digital Electronics Lab

(for an Intake of 60 Students [3 Batches])

Hardware requirement

Sl. No.	Equipment	Quantity
1	IC tester	01
2	Digital trainers	10
3	ICS-7400,7402,7404,7408,7432,7486,7483,7485,7427	25 each
4	Patch cards(different lengths)	250

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1. Construct a circuit to realize basic and universal logic gates.
2. Construct a circuit to realize NOT, OR, AND, NOR, XOR, XNOR using NAND.
3. Construct a circuit to realize NOT, OR, AND, NAND, XOR, XNOR using NOR.
4. Construct a circuit to realize half adder and full adder.
5. Construct a circuit to verify Demorgan's Theorems.
6. Construct a circuit for a given simple Boolean expression using Boolean algebra.
7. Construct a circuit to verify TT of 4:1 mux
8. Construct a circuit to verify TT 1:4 demux.
9. Construct a circuit to interface 7-segment display system with IC 7447 to display 0-9
10. Construct a circuit to verify TT of Clocked RS FF using NAND gate
11. Construct a circuit to verify TT of JK FF using IC 7476
12. Construct a circuit to verify TT of Master slave JK FF
13. Construct a circuit to verify TT of D FF
14. Construct a circuit to verify TT of Serial-in Serial-out shift register
15. Construct a circuit to verify TT of Serial-in Parallel-out shift register
16. Construct a circuit to verify TT of Parallel-in Serial-out shift register
17. Construct a circuit to verify TT of Parallel-in Parallel-out shift register
18. Construct a circuit to verify TT of 4-bit Asynchronous mod-10 (decade) counter.
19. Construct a circuit to verify TT of 4-bit synchronous up/down counter